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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,450	06/14/2006	Bartlomiej Jan Pawlak	NL031496	6828

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EXAMINER	
NHU, DAVID	
ART UNIT	**PAPER NUMBER**
2818	

NOTIFICATION DATE	DELIVERY MODE
07/05/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

TH

Office Action Summary	Application No.	Applicant(s)	
	10/596,450	PAWLAK ET AL.	
	Examiner	Art Unit	
	David Nhu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTIONS

Specifications

Content of Specification

1. The disclosure is objected to because of the following informalities: Field of the Invention, Description of the Related Art, and Brief Summary of the Invention are missing. Appropriate correction is required.

> **Background of the Invention**: The specification should set forth the Background of the Invention in two parts:
>
> (a) **Field of the Invention**: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."
>
> (b) **Description of the Related Art**: A description of the related art known to the applicant and including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

2. The following guidelines illustrate the preferred layout and content for patent applications. These guidelines are suggested for the applicant's use.

Arrangement of the Specifications

The following order or arrangement is preferred in framing the specification and, except for the reference to "Microfiche Appendix" and the drawings, each of the lettered items should appear in upper case, without underlining or bold type, as section headings. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) Title of the Invention.
(b) Cross-References to Related Applications.
(c) Statement Regarding Federally Sponsored Research or Development.
(d) Reference to a "Microfiche Appendix" (see 37 CFR 1.96).
(e) Background of the Invention.

1. Field of the Invention.
2. Description of the Related Art including information disclosed under 37 CFR 1.97 and 1.98.

(f) Brief Summary of the Invention.
(g) Brief Description of the Several Views of the Drawing(s).
(h) Detailed Description of the Invention.
(i) Claim or Claims (commencing on a separate sheet).
(j) Abstract of the Disclosure (commencing on a separate sheet).
(k) Drawings.
(l) Sequence Listing (see 37 CFR 1.821-1.825).

Claims Objection

3. Claim 10 is rejected by **a product-by-process claim**. See MPEP 2113.

Even through product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even through the prior product was made by a different process". In re Thorpe, 777F. 2d 695, 698 USPQ 964, 966 (Fed. Cir. 1985). See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Claims 1-4, "**the** projected range; **the** implanted pocket region; **the** moment; **the** deepest border; **the** formation of **the** implanted pocket region; **the** intended projected range" lack a clear antecedent basis.

There is no figures 7, 8 in the specifications.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Noda et al (6,432,802 B1), Mili-Strkalj et al (6,080,630).

6. **Regarding claim 1,** Noda, (see figures 10, 11a-11e, 2a-2c, 4a-4c, 6a-6c, col. 1, lines 15-67, col. 2, lines 1-20, col. 7-14, lines 1-67), teaches a method of manufacturing a semiconductor device having a field effect transistor (FET) in a semiconductor body of silicon 1, the method comprising: providing a surface thereof with a source region and a drain region 104 of a first conductivity type, which both are provided with extensions 105, and a channel region 103 of a second conductivity type opposite to the first conductivity type, between the source and drain regions, and a gate region 102 separated from the surface of the semiconductor body by a gate dielectric 101 above the channel region; forming a pocket region 106 below the extensions; wherein the pocket region 106 of the second conductivity type having a doping concentration higher than the doping concentration of the channel region; wherein the pocket region is formed by implanting heavy ions in the semiconductor body; after implanting a first annealing process at a moderate temperature, and a second annealing process with a fast ramp-up at a higher temperature, characterized in that between the two annealing processes, amorphous silicon in the semiconductor body is intentionally kept present in a surface region of the semiconductor body, which extends from the surface of the semiconductor body up to a projected range of an implanted pocket region (see figures 2c, 4c, 6c, 10, 11e).

Regarding claim 1, Milic-Strkalj, (see figures 2A-2H, 3-4, col. 4-9, lines 1-67), teaches a method of manufacturing a semiconductor device having a field effect transistor (FET) in a semiconductor body of silicon 202, the method comprising: providing a surface thereof with a source region 218 and a drain region 220 of a first conductivity type, which both are provided with extensions 212a, 212b, and a channel region of a second conductivity type opposite to the first conductivity type, between the source and drain regions, and a gate region 208 separated from the surface of the semiconductor body by a gate dielectric 206 above the channel region; forming a pocket region 222 below the extensions; wherein the pocket region of the second conductivity type having a doping concentration higher than the doping concentration of the channel region; wherein the pocket region is formed by implanting heavy ions in the semiconductor body; after implanting a first annealing process at a moderate temperature, and a second annealing process with a fast ramp-up at a higher temperature, characterized in that between the two annealing processes, amorphous silicon in the semiconductor body is intentionally kept present in a surface region of the semiconductor body, which extends from the surface of the semiconductor body up to a projected range of an implanted pocket region (see figures 2H, 4A-4B).

Regarding claims 2-10, Noda, (see figures 2a-2c, 4a-4c, 6a-6c, 10, 11a-11e), Milic-Strkalj, (see figures 2A-2H, 3-4), teach the first annealing process is stopped at a moment that re-growth of the semiconductor body; starting from a deepest border of a region comprising an amorphous silicon; at least in a region around a projected range of an implanted pocket region is applied between the first and second annealing process; the first and second annealing process having a temperature range and being a rapid thermal annealing (RTA) process; the

pocket region and the extensions of the source and drain are formed at the same stage of the manufacturing the semiconductor device; the semiconductor device comprising a FET.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Mili-Strkalj'586 is cited as of interest.

8. A shortened statutory period for response to this action is set to expired 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see 710.02 (b)).

9. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu, (571)272-1792. The examiner can normally be reached on Monday-Friday from 7:00 AM to 5:30 PM.

The fax phone number for the organization where this application or proceeding is assigned is (571)273-8300.

Information regarding the status of an application may be obtained from the patent application information retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Nhu

June 28, 2007